patenably distinguishing features of the present invention as claimed over the cited prior art. The present invention discloses a novel arrangement of process control modules (PCMs) applicable in IC fabrication where a wafer has a multitude of chips, of which chips each one of a given number of chips is situated in one of a multitude of adjacent exposure fields. In particular, as taught by the present invention, the given areas in which the process control modules are each arranged are formed by the exposure fields, and each process control module takes the place of at least one chip, as defined in independent claim 1. This solves the problems existing in the prior art in the circumstance where the wafer has multitude of chips, where, as explained in detail in page 1 of the Specification, there is no sufficient number of process control modules if they are located in the drop-in areas having alignment markers, or the dicing paths of the wafer have to be comparatively wide if the process control modules are located in the dicing paths.

Applicants do not agree with the assertion of the Examiner that claim 1 has been anticipated by Have patent (US Patent No. 5,128,737). Have discloses a technique to improve yield of a microelectronic integrated circuit fabrication for producing very large processor ICs where only one large circuit is realized on one wafer (see col. 14, lines 20-22). This is different from the wafer of the present invention which has a multitude of chips, of which chips each one of a given number of chips is situated in one of a multitude of adjacent exposure fields (as defined in claim 1). Due to its single large IC nature, the wafer in Have does not have the problems existing in the wafer having multitude of small chips as explained in the preceding paragraph. In fact, the processor control modules 6 in Have patent are simply located within the single chip, such as shown in Figure 1, which have less significance as compared to the large area of the whole chip. Here, it shall be pointed out that the processor control modules 6 in Have patent, but not the processor 02, shall be read as the processor control modules in the present invention (see col. 15, lines 8-16). Furthermore, the applicants respectfully disagree with Examiner's reading of the memory sub-circuits 03 in Figure 1 of Have

patent as the chips 5 in the present invention, since the whole wafer 01 in the Have patent is actually a single chip. Because of the above reasons, it is simply impossible to find, in the Have patent, any teaching or implication of the inventive features of the present invention that "the given areas in which the process control modules are each arranged are formed by the exposure fields, and each process control module takes the place of at least one chip" as defined in claim 1, which would be meaningless if applied to the single chip wafer in Have patent.

Therefore, the applicants believe claim 1 is not anticipated by the Have patent under 35 USC §102 (b), and are thus patentable. At least for the same reasons, dependent claims 2-4 are also patentable as each includes all the limitations in claim 1.

Applicants therefore respectfully request for reconsideration and allowance in view of the above remarks and amendments. The Examiner is authorized to deduct additional fees believed due from, or credit any overpayment to our Deposit Account No. 11-0223.

Respectfully submitted,

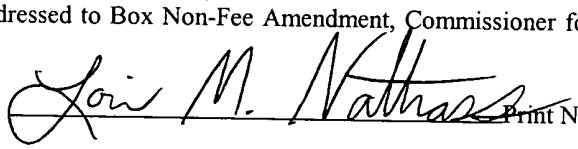
KAPLAN & GILMAN, L.L.P.
900 Route 9 North
Woodbridge, New Jersey 07095
Telephone (732) 634-7634

Dated: April 10, 2003

Jeffrey I. Kaplan
(Reg. No. 34,356)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Box Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231 on April 10, 2003.

Dated April 10, 2003 Signed  Print Name Lori M. Nattrass

MARKED-UP VERSION OF THE AMENDED SPECIFICATION AND ABSTRACT

IN THE SPECIFICATION:

Page 4, paragraph 2 (lines 3-6):

In English-language jargon such exposure fields are referred to as "reticles". In the present case, the semiconductor wafer 1 has two so-called drop-in areas **3**, which in known manner serve for positioning the semiconductor wafer 1 and at least one exposure mask during the fabrication of the semiconductor wafer 1.

IN THE ABSTRACT:

A semiconductor wafer (1) has a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2), and further has process control modules (4) which are each arranged in an exposure field (2), namely each in place of at least one chip (5).

[Figure 2.]